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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,739	01/16/2002	Matthew M. Borg	10010697	8645

57299 7590 04/06/2007

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EXAMINER	
QUIETT, CARRAMAH J	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/051,739	BORG, MATTHEW M.	
	Examiner	Art Unit	
	Carramah J. Quiett	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims 14

4)☒ Claim(s) *1-6 and ~~1~~ 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2* is/are allowed.

6)☒ Claim(s) *1,3-6 and 14-20* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment(s), filed on 01/11/2007, have been entered and made of record. Claims 1-6 and 14-21 are pending.

Response to Arguments

2. Applicant's arguments filed 01/11/2007 have been fully considered but they are not persuasive.

For claim 1, the applicant asserts that Kuroda does not disclose that reference signal Vref is a ground reference reset voltage. Respectfully, the examiner disagrees. Kuroda inherently discloses a ground reference reset voltage. In fig. 5, Kuroda illustrates Vref (85 and 86), which is a reference signal for resetting the circuit in col. 11, lines 4-15, Kuroda teaches, "Reference numeral 86 denotes a reference voltage (0V) *of the* reference signal 85." Based on the teaching and illustration of Kuroda, Vref has two points – a point where signal (85) is at a voltage greater than zero and another point at 0V (86). Signal (85) is referenced from voltage (86). Those skilled in the art would know that 0V (86) is also ground. Therefore, Kuroda discloses a ground reference reset voltage. Accordingly, the examiner maintains the rejections to claims 1, 5-6, and 14.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1, 5-6, 14** rejected under 35 U.S.C. 102(e) as being anticipated by Kuroda (U.S. Pat. #6,469,740).

For **claim 1**, Kuroda discloses an image capture system (fig. 4-5) comprising,

a plurality of rows of pixels (fig.4, Rows – (n+1), n, (n-1)), each row comprising:

a reset line for providing a reset signal (lines connected between transistors 73-76; col. 10, lines 36-39);

a plurality of pixels (23; col. 7, lines 8-10; col. 10, lines 25-29) comprising:

a first FET (76) having a gate terminal coupled to the reset line (col. 10, lines 36-57), a drain terminal coupled to a supply voltage (29,V_{ss}; col. 8, lines 5-6; col. 10, lines 44-47), and a source terminal coupled to a readout node (col. 10, lines 43-79) See fig. 4; and

a photodetector coupled (24) between a first ground (col. 7, lines 8-10; col. 10, lines 25-29) and the readout node (col. 8, lines 1-19; col. 10, lines 36-79);

a switching device (21/34/34) selectively coupled to one of the reset lines in the rows of pixels (col. 7, lines 47-63 and see fig. 4); and

a reference voltage source (72/86, V_{ref}) inherently coupled between a second ground* and one of the reset lines via the switching device (col. 10, lines 36-57; col. 11, lines 1-15), wherein the reference voltage source generates a ground referenced reset voltage (col. 11, lines 1-15 and 33-40) and the first and second grounds inherently have the same potential (col. 11, lines 1-15).

***Note:** This is inherent because in col. 11, lines 1-15, Kuroda states that the reference voltage in fig. 5 is zero volts.

For **claim 5,** Kuroda further discloses an image capture system comprising a second FET (22) having a gate terminal coupled to the readout node and a drain terminal coupled to the supply voltage. Please read col. 7, lines 47-63 and see fig. 4.

For **claim 6**, Kuroda further discloses an image capture system comprising a third FET (75) having a gate terminal coupled to a row select line, a source terminal coupled to a column line, and a drain terminal coupled to a source terminal of the second FET (col. 10, lines 36-79) See fig. 4.

For **claim 14**, Kuroda discloses the image capture system wherein the switching device comprises a multiplexer (col. 7, lines 47-63 and see fig. 4).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Kuroda (U.S. Pat. #6,469,740).

For **claim 3**, Kuroda discloses an image capture system comprsing a first FET (76) (col. 10, lines 36-57). Kuroda teaches that the *source* of the first FET (76) is connected to the gate of the pixel reset transistor (75) and the *drain* is connected to the column reset transistor (70) and the *gate* is connected to the gate of feedback row selection transistor (74). Although fig. 4 illustrates the structure of an n-channel enhancement mode MOSFET, Kuroda does not expressly teach that the first FET (76) further comprises an n-channel enhancement mode MOSFET.

Examiner takes Official Notice that it is well known in the art to have an image capture system wherein the first FET further comprises an n-channel enhancement mode MOSFET. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first FET of Kuroda with an n-channel enhancement mode MOSFET. This modification would provide the image capture system with a sub-threshold mode where voltage applied to the gate increases the current flow from source to drain. *It is noted by the Examiner that because Applicant failed to timely traverse the old and well-known statement, it is now taken as Admitted Prior Art (see MPEP 2144.03(c)).*

7. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Kuroda (U.S. Pat. #6,469,740) in view of Suzuki (U.S. Pat. #6,002,123).

For **claim 4**, Kuroda does not expressly discloses an image capture system wherein the reset voltage is greater than the supply voltage.

In the same field of endeavor, Suzuki teaches an image capture system wherein the reset voltage is greater than the supply voltage (Suzuki, figs. 3-4; col. 4, lines 40-52).. In light of the teaching of Suzuki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sensor of Kuroda with reset voltage greater than the supply voltage in order to prevent blooming thereby expanding the image sensor's dynamic range (Suzuki, col. 4, lines 31-39).

8. **Claims 15-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhuse et al. (U.S. Pat. #6,133,862) in view of Kuroda (U.S. Pat. #6,469,740).

For **claim 15**, Dhuse discloses a method comprising:

- providing a first reset (V_{reset1}) signal to a row of pixels (col. 6, line 65 – col. 7, line 9), the first reset signal being derived from a reference voltage (col. 7, lines 46-51);
- resetting pixels in the row of pixels (col. 6, line 65 – col. 7, line 9) in response to the first reset signal (V_{reset1}) using a supply voltage, the supply voltage being different from the reference voltage;

  In col. 7, lines 45-51, Dhuse teaches that the sensor array is reset to a value of V_{reset}, which is approximately the supply voltage (V_{reset} approximately V_{cc}-V_{TM1}; col. 5, line 19 – 24);
- reading a first plurality of voltage values generated at the pixels following a light exposure interval (col. 5, line 57 – col. 6, line 1; col. 6, line 65 – col. 7, line 9);
- providing a second reset signal (V_{reset2}) to the row of pixels (col. 6, line 65 – col. 7, line 9), the second reset signal being derived from the reference voltage (col. 7, lines 54-56);
- reading a second voltage value from the pixel (col. 7, lines 56-59); and
- generating a plurality of pixel values using the first and the second pluralities of voltage values (col. 6, line 65 – col. 7, line 9; col. 7, lines 51-54 and 59-67).

However, Dhuse does not teach a ground referenced reset voltage that is independent of a supply voltage. The Examiner takes Official Notice that is it well known in the art for a reference voltage source to generate a ground reference reset voltage. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sensor of Dhuse with a reference voltage source to generate a ground reference reset voltage.

This modification provides high-accuracy feedback for removing noise in image signals. *It is noted by the Examiner that because Applicant failed to timely traverse the old and well-known statement, it is now taken as Admitted Prior Art (see MPEP 2144.03(c)).*

In the same field of endeavor, Kuroda teaches a reference voltage that is independent of a supply voltage (figs. 1-3; col. 8, lines 20-50). In light of the teaching of Kuroda, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sensor of Dhuse with a reference voltage that is independent of a supply voltage in order to achieve stable operations (Kuroda, col. 8, lines 41-50).

For **claim 16**, Dhuse, as modified by Kuroda, further discloses a method wherein the plurality of pixel values equal the corresponding second plurality of voltage values minus the corresponding first plurality of voltage values (Dhuse, col. 7, lines 59-66).

For **claim 17**, Dhuse, as modified by Kuroda, further discloses a method wherein the first plurality of voltage values are approximately proportional to light intensities detected by the pixels during the light exposure interval (Dhuse, col. 5, line 57 – col. 6, line 9).

For **claim 18**, Dhuse, as modified by Kuroda, further discloses a method comprising repeating the providing a first reset signal, reading a first plurality of voltage values, providing a second reset signal, reading, and generating a plurality of pixel values for another row of pixels (Dhuse, col. 7, lines 45-67).

For **claim 19**, Dhuse, as modified by Kuroda, further discloses a method wherein the generating is performed by a column circuit (Dhuse, col. 7, lines 10-35).

For **claim 20**, Dhuse, as modified by Kuroda, further discloses a method wherein the reading a first plurality of voltage values comprises exposing photodiodes to incident light (Dhuse, col. 4, lines 7-22).

Allowable Subject Matter

9. **Claim 2** is allowed.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claim 2 is allowed because the prior art does not teach or fairly suggest the image capture system, comprising: an operational amplifier buffer comprising (1) an output coupled by the switching device to one of the reset lines (2) *a non-inverting input coupled to the reference voltage source to receive the reset voltage, and (3) an inverting input coupled to the output in a feedback loop, wherein the feedback loop does not pass through the readout node.*

11. **Claim 21** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claim 21 is allowed because the prior art does not teach or fairly suggest the image capture system of claim 6, further comprising an operational amplifier comprising (1) an output coupled by the switching device to one of the reset lines, *(2) a non-inverting input coupled to the reference voltage source to receive the reset voltage, and (3) an inverting input coupled to the output in a feedback loop, wherein the feedback loop does not pass through the readout node.*

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CJQ
March 26, 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER